

FIG. 1

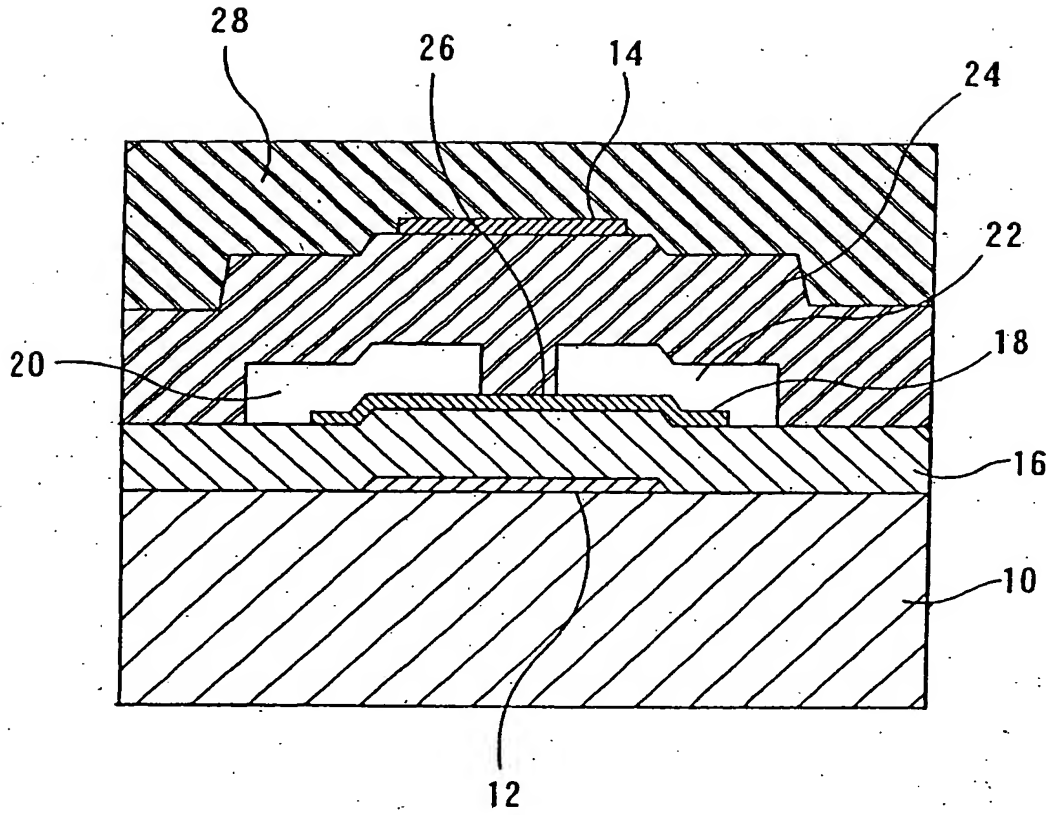
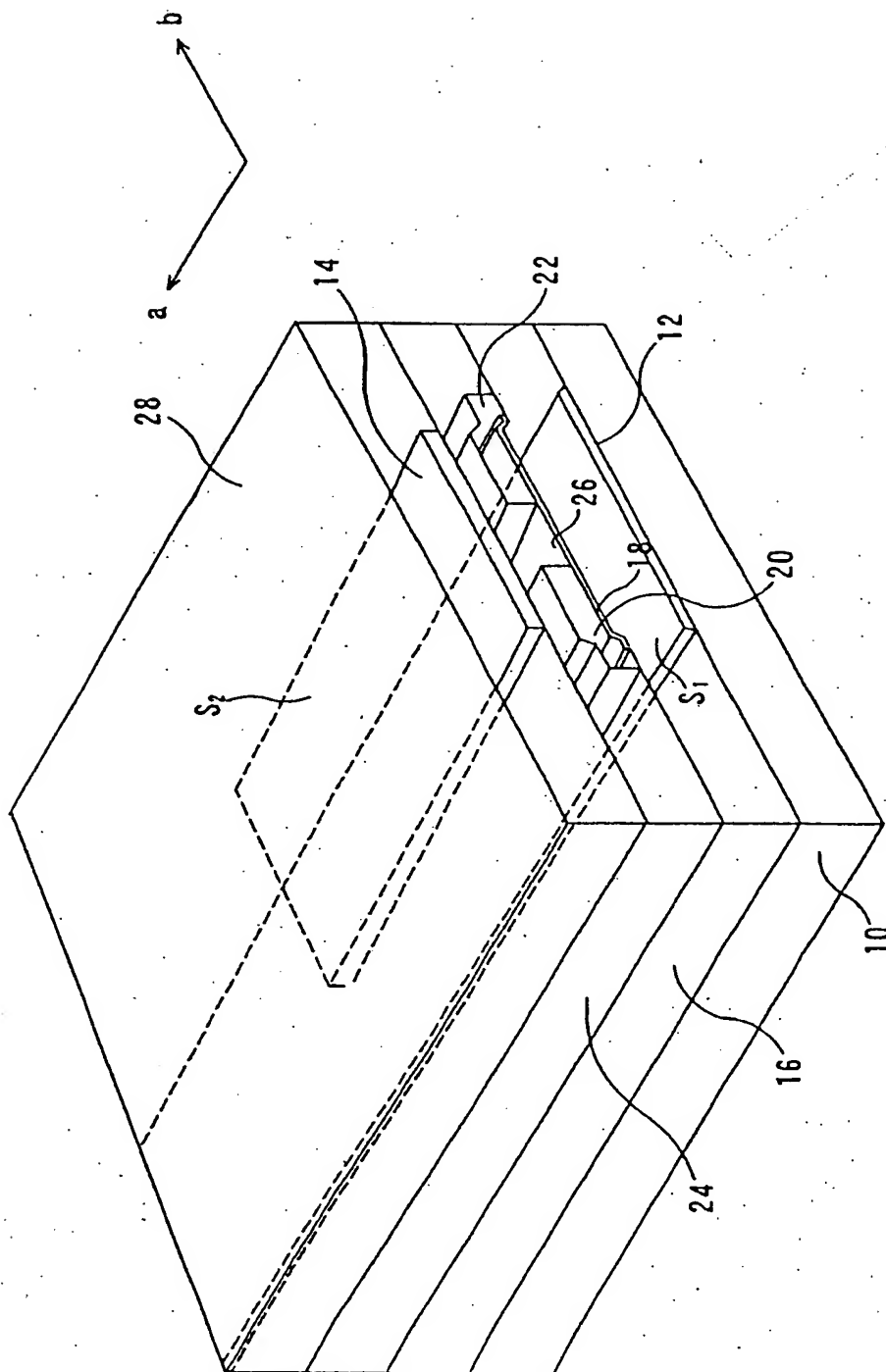


FIG. 2



This cross-sectional view shows a semiconductor device with three distinct gate regions labeled 36, 32, and 34. Region 36 includes a gate stack 46, a gate 42, and a gate 36b. Region 32 includes a gate 14. Region 34 includes a gate 34b, a gate 44, and a gate 48. The device is built on a substrate 10, with a base layer 12, a channel layer 16, and a drift layer 24. A top layer 28 is also present. The gate regions are separated by spacers 36a, 36c, 34a, and 34c.

FIG. 5

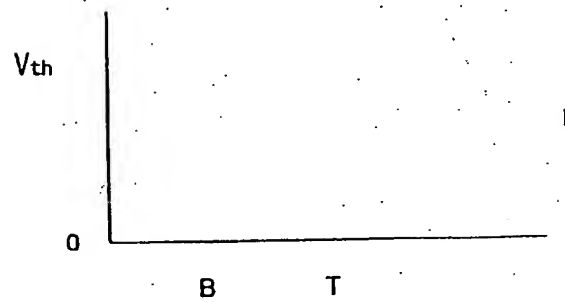
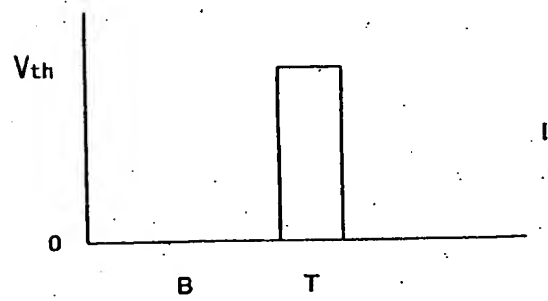
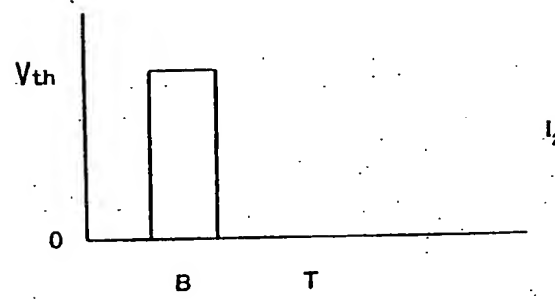
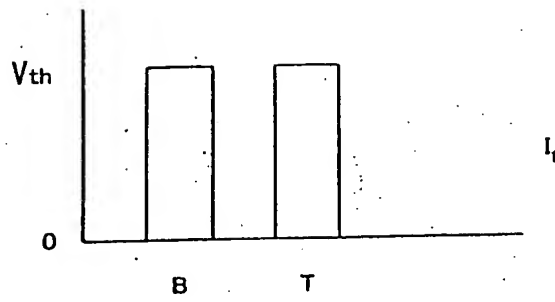


FIG. 6

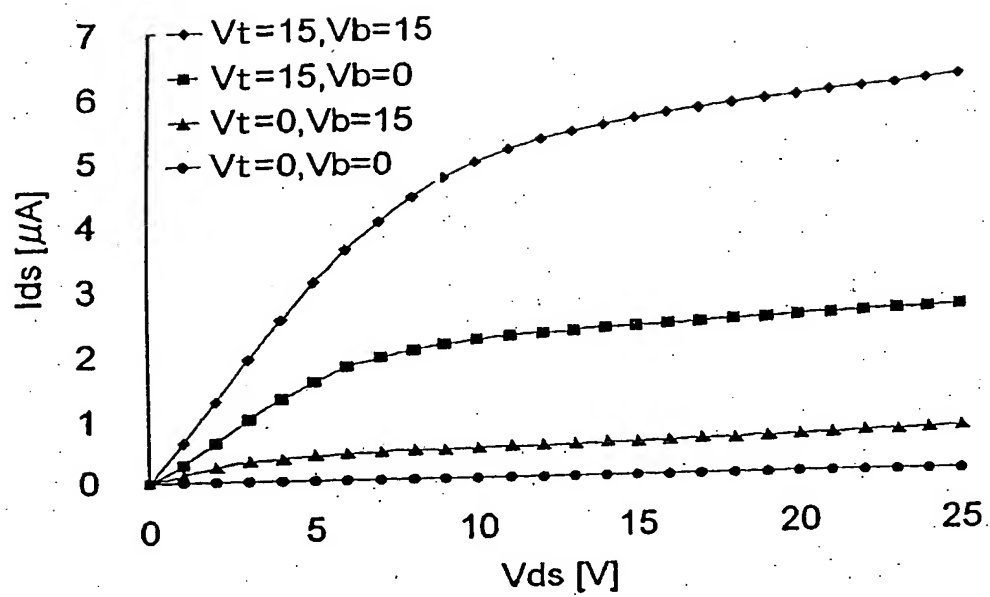
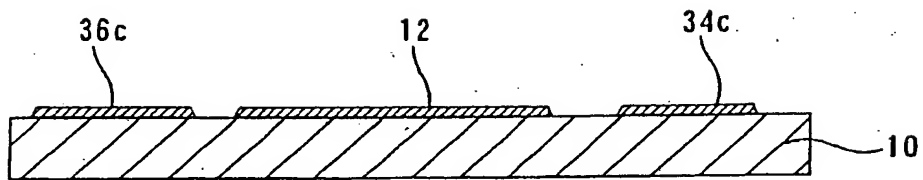
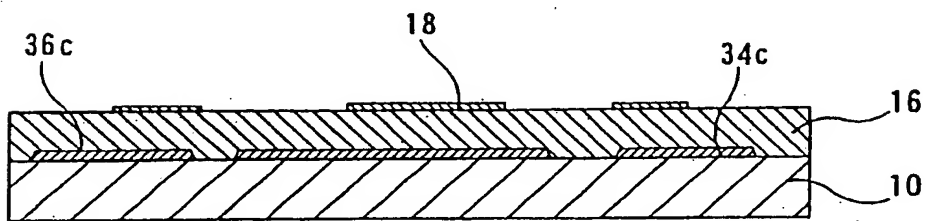


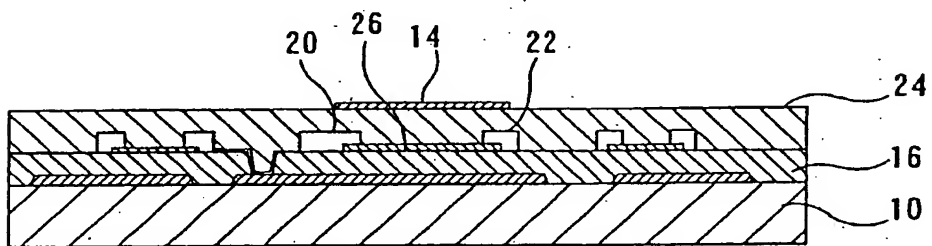
FIG. 7



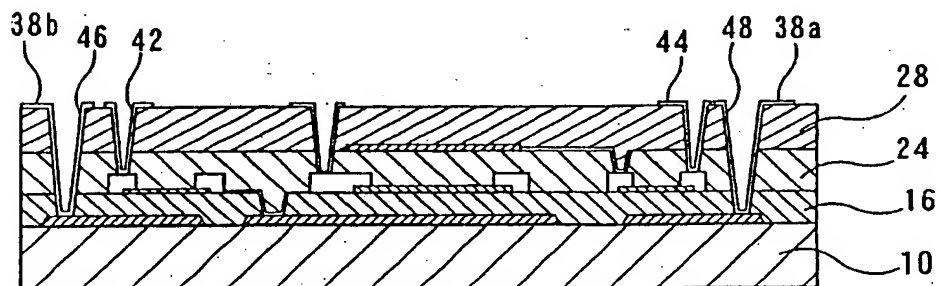
(a)



(b)



(c)



(d)

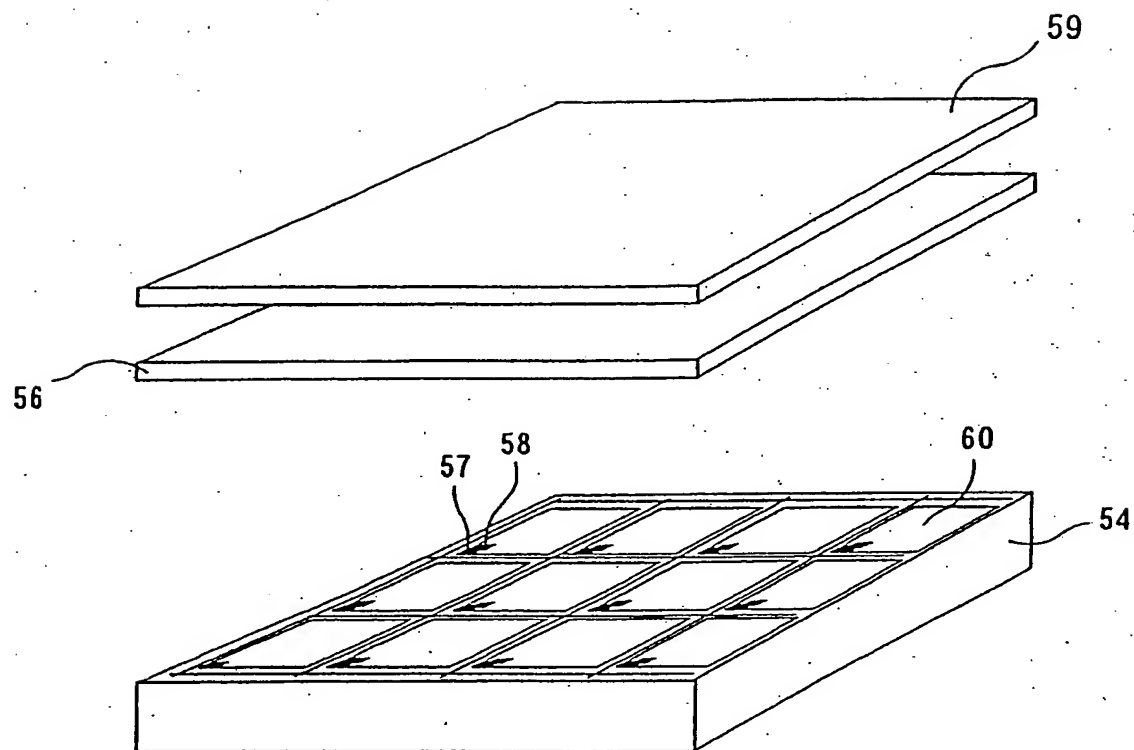


FIG. 9

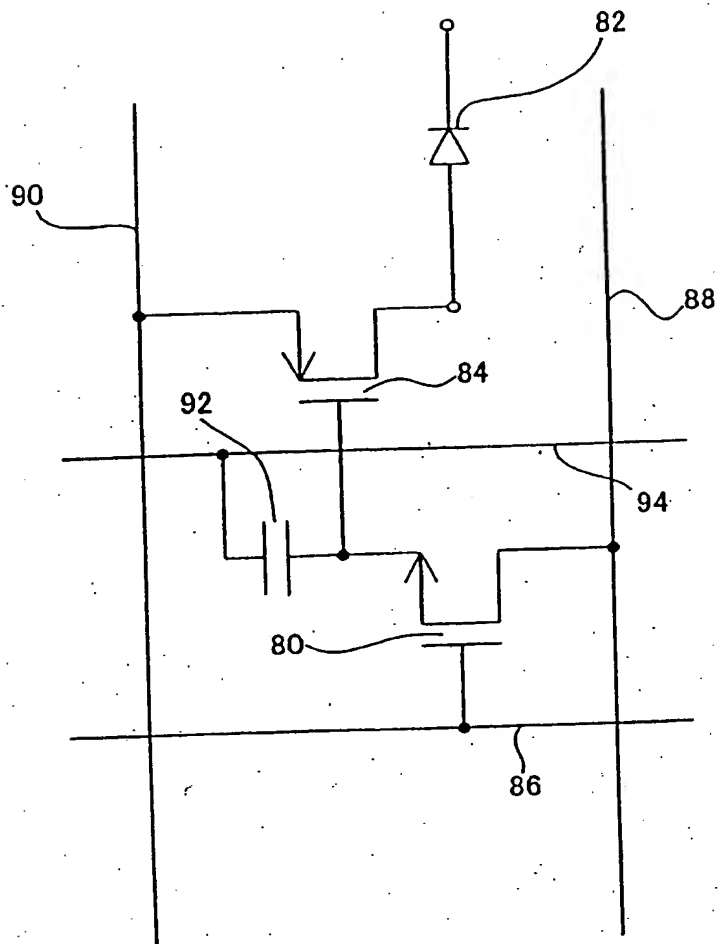


FIG. 10

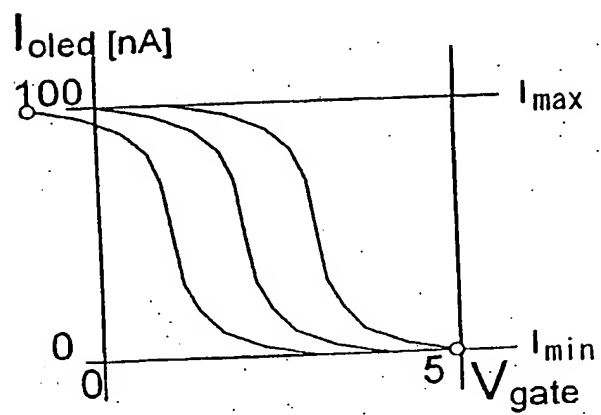


FIG. 11

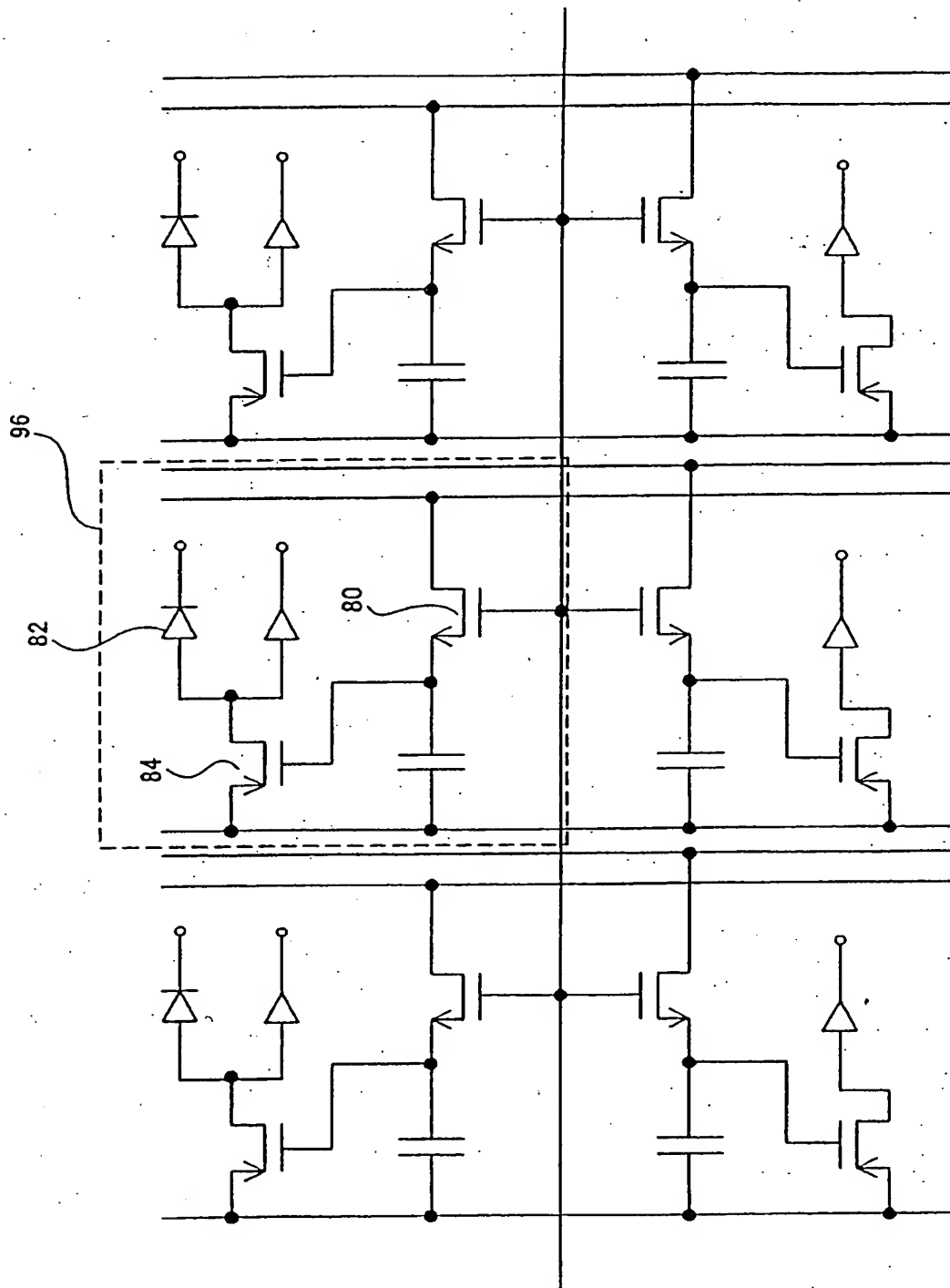


FIG. 12

